UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,322	12/18/2001	Naoto Kusumoto	07977/076003/US3130/3134D	8044

26171 7590 02/07/2005

FISH & RICHARDSON P.C.
1425 K STREET, N.W.
11TH FLOOR
WASHINGTON, DC 20005-3500

EXAMINER
MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,322	KUSUMOTO ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 16-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 16-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20041207*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funai et al. (U.S. 6,162,667) in view of Ghandhi et al. (VLSI Fabrication Principles).

In reference to claim 1, Funai et al. (Figs.19A-19E) teach a method of forming a semiconductor device including the steps of forming a semiconductor film (1302) over a substrate (1300); first cleaning a surface of the semiconductor film by using a first solution (column 44, lines 58 – 67 and column 45, lines 40 – 48); applying a laser beam to the cleaned surface of said semiconductor film (1302) to increase crystalinity of the semiconductor film (1302) (column 45, lines 40 – 48); patterning the semiconductor film (1302); and forming a gate insulating film (1306) on a surface of the patterned semiconductor film (1302i) (column 44, line 50 – column 46, line 49).

Funai et al. fail to teach second cleaning a surface of the semiconductor film by using a second solution after applying the laser beam; and patterning the semiconductor film after the second cleaning. However, Ghandhi et al. teach that is common practice in the art to clean the semiconductor wafer after each step during the fabrication of semiconductor device in order to avoid operation error (Ghandhi et al.,

page 517 – page 520). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Funai et al. and Ghandhi et al. to enable performing a cleaning step after each step in the process of Funai et al. as taught by Ghandhi et al.

In reference to claim 2, the combined teachings of Funai et al. and Ghandhi et al. teach wherein said first cleaning solution comprises HF aqueous solution of an aqueous solution containing HF and H_2O_2 (Funai et al. column 44, lines 58 – 67 and Ghandhi et al., page 517 – page 520).

In reference to claim 3, the combined teachings of Funai et al. and Ghandhi et al. substantially teach all aspects of the invention including wherein said laser has an energy density of 200 to 400 mJ/cm^2 (Funai et al., column 45, lines 39 – 47), but fail to disclose wherein said laser beam has an energy density of 100 to 500 mJ/cm^2. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the laser energy range disclosed in the combined teachings of Funai et al. and Ghandhi et al. to arrive at the claimed invention.

In reference to claims 29 and 30, the combined teachings of Funai et al. and Ghandhi et al. teach wherein the cleaning solutions are either different or the same (Funai et al. column 44, lines 58 – 67 and Ghandhi et al., page 517 – page 520).

3. Claims 4-6, 10-12 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funai et al. (U.S. 6,162,667) in view of Ramesh et al. (U.S. 4,795,679).

In reference to claims 4, 10 and 16, Funai et al. (Figs.19A-19E) teach a method of forming a semiconductor device including the steps of forming a semiconductor film (1302) over a substrate (1300); cleaning a surface of the semiconductor film (1302) by using a cleaning solution (column 44, lines 58 – 67 and column 45, lines 40 – 48); preheating the cleaned surface of said semiconductor film to form a capping oxide film (1303); applying a heating step to said semiconductor film (1302) to crystallize said film; removing said oxide film (1303); applying a laser beam to said semiconductor film (1302) to increase crystalinity of the semiconductor film (1302); and patterning the semiconductor film (1302) after applying the laser beam (column 44, line 50 – column 46, line 49). Furthermore, Funai et al. teach applying a laser beam through an oxide layer to improve crystalinity after patterning said semiconductor film (1302) (column 46, lines 39 – 49).

Still Funai et al. fail to teach applying a laser beam to said semiconductor film through an oxide layer to improve crystalinity. However, Ramesh et al. teach a method of forming a semiconductor device, including forming a semiconductor film on a substrate; forming a dielectric capping layer on top of said semiconductor film; and annealing said semiconductor film by laser beam to said semiconductor film through said dielectric capping layer, wherein said capping layer acts to prevent agglomeration

of semiconductor during crystallization and to prevent contamination of the semiconductor during crystallization (column 1, lines 17 – 54).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Funai et al. and Ramesh to enable providing a dielectric capping layer as taught by Funai et al. during the laser annealing in Funai et al. since, as taught by Ramesh et al., it would prevent agglomeration of semiconductor during crystallization and to prevent contamination of the semiconductor during crystallization (Ramesh et al., column 1, lines 17 – 54).

In reference to claims 5, 11 and 17, the combined teachings of Funai et al. and Ramesh et al. teach wherein said cleaning solution comprises HF aqueous solution of an aqueous solution containing HF and H_2O_2 (Funai et al. column 44, lines 58 – 67).

In reference to claims 6, 12 and 18, the combined teachings of Funai et al. and Ramesh et al. substantially teach all aspects of the invention including wherein said laser has an energy density of 200 to 400 mJ/cm^2 (Funai et al., column 45, lines 39 – 47), but fail to disclose wherein said laser beam has an energy density of 100 to 500 mJ/cm^2. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the laser energy range disclosed in the combined teachings of Funai et al. and Ramesh et al. to arrive at the claimed invention.

4. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funai et al. (U.S. 6,162,667) in view of Yoneda (U.S. 5,648,282) and Ramesh et al. (U.S. 4,795,679).

Funai et al. (Figs.19A-D) in a related method to form a crystalline semiconductor film structure teach forming an amorphous silicon film (1302) over a substrate (1301, 1300); cleaning a surface of the silicon film (1302) by using HF aqueous solution; preheating said silicon film (1302) to form an oxide film (1303); applying a first heat treatment to the silicon film (1302) having said oxide film (1303) formed thereon thus forming a crystallizing said silicon film; cleaning the surface of the crystallized silicon film; and applying second heat treatment consisting of a laser beam to said semiconductor film to improve the crystalinity of the semiconductor film (1302a), said laser beam in an inert atmosphere applied at an energy density of 200 to 400 mJ/cm^2 (column 44, line 41 – column 45, line 48). Furthermore, Funai et al. teach forming an oxide layer (1306) over the crystallized silicon film; implanting dopants through the oxide layer (1306) into the crystallized silicon film, wherein said implantation deteriorates the crystalinity of said silicon film; and performing a third heat treatment consisting of a laser beam (1312) in an inert atmosphere to said deteriorated silicon film through said oxide layer (1306) to activate implanted dopants and to improve the crystalinity of said deteriorated silicon film at an energy of 200 to 250 mJ/cm^2 (column 45, line 57 – column 46, line 49).

Funai et al. fail to teach preheating said semiconductor film in an atmosphere containing oxygen and nitrogen. However, Yoneda (Fig.1A) in a related method to form

an oxide layer teaches heating a semiconductor substrate (101) in an atmosphere containing oxygen and nitrogen environment to form and oxide film over a region (110) in the semiconductor substrate (101) (column 11, line 53 – column 12, line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to perform the heating process in an oxygen and nitrogen atmosphere as taught by Yoneda in the crystalline semiconductor film process of Funai et al., since this would result in the formation of an oxide layer in a purged environment (column 11, line 53 – column 12, line 5).

Still, the combined teachings of Funai et al. and Yoneda fail to teach wherein said laser beam has an energy density of 100 to 500 mJ/cm^2. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the laser energy range disclosed in the combined teachings of Funai et al. and Hoga to arrive at the claimed invention.

Furtherstill, the combined teachings of Funai et al. and Yoneda fail to teach applying a laser beam to said semiconductor film through an oxide layer to improve crystalinity. However, Ramesh et al. teach a method of forming a semiconductor device, including forming a semiconductor film on a substrate; forming a dielectric capping layer on top of said semiconductor film; and annealing said semiconductor film by laser beam to said semiconductor film through said dielectric capping layer, wherein said capping layer acts to prevent agglomeration of semiconductor during crystallization

and to prevent contamination of the semiconductor during crystallization (column 1, lines 17 – 54).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Funai et al. and Yoneda with Ramesh et al. to enable providing a dielectric capping layer as taught by Funai et al. and Yoneda during the laser annealing in Funai et al. and Hoga since it would prevent agglomeration of semiconductor during crystallization and to prevent contamination of the semiconductor during crystallization (Ramesh et al., column 1, lines 17 – 54).

5. Claims 19-26 and 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funai et al. (U.S. 6,162,667) in view of Ramesh et al. (U.S. 4,795,679), Ghandhi et al. (VLSI Fabrication Principles) and Asai et al. (U.S. 5,365,875).

In reference to claims 19, 20, 23 and 24, Funai et al. (Figs.19A-19E) teach a method of forming a semiconductor device including the steps of forming a semiconductor film (1302) over a substrate (1300); cleaning a surface of the semiconductor film (1302) by a cleaning solution that includes HF (column 44, lines 58 – 67 and column 45, lines 40 – 48); preheating the cleaned surface of said semiconductor film to form a capping oxide film (1303); applying a heating step to said semiconductor film (1302) to crystallize said film; removing said oxide film (1303); applying a laser beam to said semiconductor film (1302) to increase crystalinity of the semiconductor film (1302); and patterning the semiconductor film (1302) after applying the laser beam (column 44, line 50 – column 46, line 49). Furthermore, Funai et al. teach applying a

laser beam through an oxide layer to improve crystalinity after patterning said semiconductor film (1302) (column 46, lines 39 – 49).

Still Funai et al. fail to teach applying a laser beam to said semiconductor film through an oxide layer to improve crystalinity. However, Ramesh et al. teach a method of forming a semiconductor device, including forming a semiconductor film on a substrate; forming a dielectric capping layer on top of said semiconductor film; and annealing said semiconductor film by laser beam to said semiconductor film through said dielectric capping layer, wherein said capping layer acts to prevent agglomeration of semiconductor during crystallization and to prevent contamination of the semiconductor during crystallization (column 1, lines 17 – 54).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Funai et al. and Ramesh to enable providing a dielectric capping layer as taught by Funai et al. during the laser annealing in Funai et al. since, as taught by Ramesh et al., it would prevent agglomeration of semiconductor during crystallization and to prevent contamination of the semiconductor during crystallization (Ramesh et al., column 1, lines 17 – 54).

The combined teachings Funai et al. and Ramesh et al. fail to teach second cleaning a surface of the semiconductor film by using a second solution after applying the laser beam; and patterning the semiconductor film after the second cleaning. However, Ghandhi et al. teach that is common practice in the art to clean the semiconductor wafer after each step during the fabrication of semiconductor device in order to avoid operation error (Ghandhi et al., page 517 – page 520). Therefore, it would

have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Funai et al. and Ramesh et al. with Ghandhi et al. to enable performing a cleaning step after each step in the process of Funai et al. and Ramesh et al. as taught by Ghandhi et al.

Still, the combined teachings of Funai et al., Ramesh et al. and Ghandhi et al. fail to teach performing the laser annealing in air. However, Asai et al. (Figs.2a-2d) in a related method to form a crystalline semiconductor film teach applying a laser beam to a semiconductor layer (2) forming a crystalline semiconductor layer (2') in air (column 10, line 20 – column 11, line 3). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Funai et al., Ramesh et al. and Ghandhi with the teachings of Asai et al. to enable the annealing step of Funai et al., Ramesh et al. and Ghandhi et al. to be performed according to the teachings of Asai et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed annealing step of Funai et al., Ramesh et al. and Ghandhi et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claims 21, 22, 25 and 26, the combined teachings of Funai et al., Ramesh et al., Ghandhi et al. and Asai et al. substantially teach all aspects of the invention including wherein said laser has an energy density of 200 to 400 mJ/cm^2 and said oxide layer can have a thickness of 10-20Å (Funai et al., column 45, lines 1 – 2 and lines 39 – 47), but fail to disclose wherein said laser beam has an energy density of 100 to 500 mJ/cm^2 and said oxide film has a thickness of 20-40Å. However, in the case

where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the laser energy range and the thickness range disclosed in the combined teachings of Funai et al. and Ramesh et al. to arrive at the claimed invention.

In reference to claims 36-39, the combined teachings of Funai et al., Ramesh et al., Ghandhi et al. and Asai et al. teach wherein the cleaning solutions are either different or the same (Funai et al. column 44, lines 58 – 67 and Ghandhi et al., page 517 – page 520).

6. Claim 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Funai et al. (U.S. 6,162,667) in view of Ghandhi et al. (VLSI Fabrication Principles) as applied to claims 1-3, 29 and 30 above, and further in view of Hoga (U.S. 4,552,595).

The combined teachings of Funai et al. and Ghandhi et al. substantially teach all aspects of the invention but fail to disclose wherein the laser beam comprises doing so in a nitrogen atmosphere. However, Hoga (Figs.2A-2B) in a related method to form a crystalline semiconductor structure teaches providing a silicon substrate (11); implanting ions into said substrate (11), thus forming an amorphous silicon layer (12); forming a second amorphous silicon layer (13); and performing a heating process by applying a laser in a nitrogen atmosphere to form a crystalline semiconductor film (14) (column 2, lines 53 – 61). It would have been obvious to combine the teachings of Funai et al. and Ghandhi et al. with Hoga to enable performing the heating processes of Funai et al.

using the laser anneal process as taught by Hoga, since this would result in the formation of a polycrystalline region in an inert atmosphere (column 2, lines 53 – 61) with reduced impurities. It would also have been obvious to one of ordinary skill in the art at the time the invention was made to enable performing all of the heating process disclosed in the combined teachings of Funai et al., Ghandhi et al. and Hoga to arrive at the claimed invention.

7. Claim 28 rejected under 35 U.S.C. 103(a) as being unpatentable over Funai et al. (U.S. 6,162,667) in view of Ghandhi et al. (VLSI Fabrication Principles) as applied to claims 1-3, 29 and 30 above, and further in view of Asai et al. (U.S. 5,365,875).

The combined teachings of Funai et al. and Ghandhi et al. fail to teach performing the laser annealing in air. However, Asai et al. (Figs.2a-2d) in a related method to form a crystalline semiconductor film teach applying a laser beam to a semiconductor layer (2) forming a crystalline semiconductor layer (2') in air (column 10, line 20 – column 11, line 3). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Funai et al. and Ghandhi with the teachings of Asai et al. to enable the annealing step of Funai et al. and Ghandhi et al. to be performed according to the teachings of Asai et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed annealing step of Funai et al. and Ghandhi et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

8. Claims 31 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funai et al. (U.S. 6,162,667) in view of Ramesh et al. (U.S. 4,795,679) as applied to claims 4-6, 10-12 and 16-18 above, and further in view of Hoga (U.S. 4,552,595).

The combined teachings of Funai et al. and Ramesh et al. substantially teach all aspects of the invention but fail to disclose wherein the laser beam comprises doing so in a nitrogen atmosphere. However, Hoga (Figs.2A-2B) in a related method to form a crystalline semiconductor structure teaches providing a silicon substrate (11); implanting ions into said substrate (11), thus forming an amorphous silicon layer (12); forming a second amorphous silicon layer (13); and performing a heating process by applying a laser in a nitrogen atmosphere to form a crystalline semiconductor film (14) (column 2, lines 53 – 61). It would have been obvious to combine the teachings of Funai et al. and Ramesh et al. with Hoga to enable performing the heating processes of Funai et al. using the laser anneal process as taught by Hoga, since this would result in the formation of a polycrystalline region in an inert atmosphere (column 2, lines 53 – 61) with reduced impurities. It would also have been obvious to one of ordinary skill in the art at the time the invention was made to enable performing all of the heating process disclosed in the combined teachings of Funai et al., Ramesh et al. and Hoga to arrive at the claimed invention.

9. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funai et al. (U.S. 6,162,667) in view of Yoneda (U.S. 5,648,282) and Ramesh et al. (U.S. 4,795,679) as applied to claims 7-9 above, and further in view of Hoga (U.S. 4,552,595).

The combined teachings of Funai et al., Yoneda and Ramesh et al. substantially teach all aspects of the invention but fail to disclose wherein the laser beam comprises doing so in a nitrogen atmosphere. However, Hoga (Figs.2A-2B) in a related method to form a crystalline semiconductor structure teaches providing a silicon substrate (11); implanting ions into said substrate (11), thus forming an amorphous silicon layer (12); forming a second amorphous silicon layer (13); and performing a heating process by applying a laser in a nitrogen atmosphere to form a crystalline semiconductor film (14) (column 2, lines 53 – 61). It would have been obvious to combine the teachings of Funai et al., Yoneda and Ramesh et al. with Hoga to enable performing the heating processes of Funai et al. using the laser anneal process as taught by Hoga, since this would result in the formation of a polycrystalline region in an inert atmosphere (column 2, lines 53 – 61) with reduced impurities. It would also have been obvious to one of ordinary skill in the art at the time the invention was made to enable performing all of the heating process disclosed in the combined teachings of Funai et al., Yoneda, Ramesh et al. and Hoga to arrive at the claimed invention.

10. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funai et al. (U.S. 6,162,667) in view of Yoneda (U.S. 5,648,282) and Ramesh et al. (U.S. 4,795,679) as applied to claims 7-9 above, and further in view of Asai et al. (U.S. 5,365,875).

The combined teachings of Funai et al. Yoneda and Ramesh et al. fail to teach performing the laser annealing in air. However, Asai et al. (Figs.2a-2d) in a related method to form a crystalline semiconductor film teach applying a laser beam to a

semiconductor layer (2) forming a crystalline semiconductor layer (2') in air (column 10, line 20 – column 11, line 3). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Funai et al., Yoneda and Ramesh et al. with the teachings of Asai et al. to enable the annealing step of Funai et al., Yoneda and Ramesh et al. to be performed according to the teachings of Asai et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed annealing step of Funai et al., Yoneda and Ramesh et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Response to Arguments

11. Applicant's arguments with respect to claims 1-12 and 16-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
February 3, 2005

George Fourson
Primary Examiner